Application No.: 09/940,324
Response dated: July 10, 2006
Reply to Office Action dated: April 10, 2006

<u>REMARKS/ARGUMENTS</u>

Claims 1-17 are pending in the application.

Claims 1-4 and 6-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over

U.S. Patent 6,526,481 to Shen et al. in view of U.S. Patent 6,859,861 to Rhodes.

The Examiner has agreed that Shen fails to disclose a plurality of sub-unit caches recited

in claims of the present application. However, the Examiner has asserted that it is well known in

the cache art to divide a cache into a plurality of sub-unit caches, referring to Rhodes.

Applicants respectfully disagree.

Shen provides a methodology for designing a memory system that incorporates

adaptation or selection of cache protocols during operation while guaranteeing semantically

correct processing of memory instructions *by multiple processors* (Shen, col. 3, lines 26-30).

Fig. 1 of Shen shows a multiple processor computer system 100 including *multiple instruction*

processors 110 coupled to a memory system 120.

However, the claimed invention solves a very different problem. Claims of the present

application recite a cache-coherent *input/output device*. As discussed in the background section

of the present application, *processors are commonly referred to as "cacheable" device, but*

input/output components are generally non-cacheable devices (Specification, page 3, lines 14-

17).

Rhodes is irrelevant to a cache-coherent input/output device as well. According to

Rhodes, although cache memories have been particularly arranged in the prior art to expedite

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computer operations, the ever increasing *speed of processors* renders it desirable to further

improve memory arrangements for expediting computer operations (Rhodes, col. 1, lines 27-31).

Thus, Shen and Rhodes concern memory for processors, but the claimed invention recites

a cache-coherent input/output device. Since the problems solved by Shen and Rhodes are very

different from recited elements of the claimed invention, there is no suggestion or motivation to

combine Shen and Rhodes to reconstruct the claimed invention.

Even assuming, *arguendo*, that a skilled artisan were to combine Shen and Rhodes, the

combination would not result in the claimed invention, since neither Shen nor Rhodes discloses a

cache coherent input/output device. Accordingly, Applicants respectfully submit that the

Examiner's combination of Shen and Rhodes is improper.

Shen discloses a methodology for designing a distributed shared-memory system. The

distributed shared-memory system can incorporate adaptation or selection of cache protocols

during operation. It guarantees semantically correct processing of memory instructions by the

multiple processors (Abstract). Shen also states:

> Referring still to FIG. 2, memory system 120 includes one cache 130
> for *each instruction processor 110,* and shared-memory system 140. Each
> cache 130 includes a cache controller 132 and a cache storage 134. Cache
> storage 134 includes data storage which associates address, data, and status
> information for a limited portion of the address space accessible from
> instruction processor 110. Cache controller 132 communicates with memory
> access unit 117. Memory access unit 117 passes memory access messages to
> cache controller 132 in response to memory access instructions issued by
> instruction pool 114. Cache controller 132 processes these memory access
> messages by accessing its cache storage 134, by communicating in turn with
> shared-memory system 140, or both. When it has finished processing a
> memory access message, it sends a result or acknowledgment back to memory

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> access unit 117, which in turn signals to instruction pool 114 that the
> corresponding memory access instruction has completed.

(Shen, col. 8, lines 45-62, emphasis added).

Thus, Shen describes using cache coherency protocols to allow a number of instruction

processors to access a distributed cache memory system and not the use of distributed caches for

cache-coherent input/output.

Rhodes discloses cache memory structures for alleviating the continually increasing

memory latency or delay problem caused by the ever increasing speed of *computer processors*

(Rhodes, Abstract). Rhodes states:

> As shown in FIG. 2, the present invention relates to a computer system 20
> wherein a plurality of separate and independent memory branches 22 extend from
> a common bus 24 that passes on a hierarchical level immediately above a
> processor 26. Each memory branch 22 is initiated with a cache memory unit 30
> and ascends hierarchically to at least one main memory unit 28. Other
> intermediate cache memory units 30 may be disposed in each branch 22 between
> the initial cache memory unit 30 and the main memory units 28. Generally, the
> addresses of the information stored in each memory branch 22 are distinctive
> relative to the addresses of the information stored in all of the other memory
> branches 22. Therefore, *when an address is applied to the common bus 24 by the*
> *processor 26, if information is stored at that address in cache memory, it is*
> *retrieved by the processor 26 from only one of the memory branches 22.* Of
> course, each cache memory unit 30 has less information storage capacity than the
> main memory unit 28 associated therewith in the memory branch 22.
> Consequently, each cache memory unit 30 may enjoy a higher hit-rate (or a lower
> miss-rate) than does the main memory unit 28 associated therewith.

(Rhodes, col. 2, lines 40-61, emphasis added).

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Thus, Rhodes fails to disclose a cache-coherent input/output device either.

Accordingly, Applicants respectfully submit that claims 1-17 are patentable over the combination of Shen and Rhodes.

Claims 5, 13 and 15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shen in view of Rhodes and further in view of Jim Handy, "The Cache Memory Handbook", TK7895.M4H35, 1993, pp 140-240.

Handy discloses a protocol for use in *multiple processor system* with multiple caches. Handy fails to teach a cache-coherent input/output device, and does not supply any deficiency of Shen or Rhodes. Accordingly, Applicants respectfully submit that claims 5, 13 and 15 are patentable over the combination Shen, Rhodes and Handy for this additional reason as well.

Claims 16 and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Shen in view of Rhodes and Handy, and further in view of Witt et al. (U.S. Patent 6,202,139).

Witt discloses a computer system including a processor having a cache which includes multiple ports. The cache is pipelined and operates at a clock frequency higher than that employed by the remainder of the microprocessor including the cache for multiple accesses per clock cycle (Witt, col. 2, lines 31-36 and Abstract). Thus, Witt fails to teach a cache-coherent input/output device and does not supply any deficiency of Shen, Rhodes, or Handy. Accordingly, Applicants respectfully submit that claims 16 and 17 are patentable over the combination of Shen, Rhodes, Handy and Witt.

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For all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited. The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to the deposit account of Kenyon & Kenyon, deposit account no. **11-0600.**

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Respectfully submitted,

KENYON & KENYON LLP

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Dated: July 10, 2006   By: _Lin Deng_

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